CLAIMS

1. A circuit comprising:

multiple components;

a plurality of clock drivers configured to provide separate clock signals to each of the components by way of separate paths; and

a phase feedback element corresponding to a pair of components, wherein the phase feedback element is configured to receive and adjust the phase of one of the clock signals, in response to the received clock signal, to more closely match the phase of the other of the clock signals.

2. The circuit of claim 1, wherein the received clock signal is routed along a received clock signal path which is located near the corresponding components.

3. The circuit of claim 1, wherein the clock signals are received at adjacent ends of the components.

4. The circuit of claim 1, wherein the separate paths have different propagation delays.

5. The circuit of claim 4, wherein the separate paths have different lengths.

6. The circuit of claim 1, wherein the phase feedback element comprises a phase comparator.

7. The circuit of claim 6, wherein:

the phase comparator is configured to determine a phase offset; and

the clock drivers are responsive to the phase offsets to adjust the phases of the clock signals.

8. The circuit of claim 7, wherein the phase offset of the phase comparator is a digital phase offset.

9. The circuit of claim 1, wherein the phase feedback element comprises a phase comparator that is responsive to the received component clock signals to adjust the phase of the one of the received clock signals to match the phase of the other of the received clock signals.

10. The circuit of claim 1, wherein the phase feedback element corresponding to the pair of the components comprises:

an integrator;

a first current source configured to be selectively enabled by the clock signal corresponding to a first of the components of the pair of components, the first current source being further configured to charge the integrator when enabled; and

a second current source configured to be selectively enabled by the clock signal corresponding to a second of the components of the pair of components, the

second current source being further configured to discharge the integrator when enabled.

11. The circuit of claim 1, wherein the phase feedback element comprises:

a capacitive element;

a first current source configured to be selectively enabled by the clock signal corresponding to a first of the component of the pair of components, the first current source being further configured to charge the capacitive element when enabled; and

a second current source configured to be selectively enabled by the clock signal corresponding to a second of the component of the pair of components, the second current source being further configured to discharge the capacitive element when enabled.

12. The circuit of claim 11, wherein at least one of the clock drivers is responsive to a voltage at the capacitive element to adjust the phase of its clock signal.

13. A circuit comprising:

multiple components;

a plurality of clock drivers configured to provide separate component clock signals to respectively corresponding components by way of separate paths;

a reference feedback element that receives a reference clock signal and a clock signal from one of the components, wherein the reference feedback element

is configured to adjust the phase of the clock signal from one of the components, in response to the reference clock signal and the received clock signal from one of the components to more closely match the phase of the reference clock signal; and

a phase feedback element corresponding to a pair of components, wherein the phase feedback element receives clock signals from each component of the pair and is responsive to the received clock signals to adjust the phase of one of the clock signals to match the phase of the other of the clock signals; wherein the clock signals received by the reference feedback element and the phase feedback element are routed from near the corresponding components.

14. The circuit of claim 13, wherein the separate paths have different propagation delays.

15. The circuit of claim 13, wherein the separate paths have different lengths.

16. The circuit of claim 13, wherein the reference feedback element and the phase feedback element comprise phase comparators.

17. The circuit of claim 13, wherein:

the reference feedback element and phase feedback elements comprise phase comparators;

each phase comparator is configured to determine a phase offset; and

the clock drivers are responsive to the phase offsets to adjust the phases of the clock signals of the components.

18. The circuit of claim 17, wherein the phase offset is a digital phase offset.

19. The circuit of claim 13, wherein the phase feedback element comprises:

an integrator;

a first current source configured to be selectively enabled by the clock signal corresponding to a first component of the pair of components, the first current source being further configured to charge the integrator when enabled; and

a second current source configured to be selectively enabled by the clock signal corresponding to a second component of the pair of components, the second current source being further configured to discharge the integrator when enabled.

20. The circuit of claim 13, wherein the phase feedback element comprises:

a capacitive element;

a first current source configured to be selectively enabled by the clock signal corresponding to a first component of the pair of components, the first current source being further configured to charge the capacitive element when enabled; and

a second current source configured to be selectively enabled by the clock signal corresponding to a second component of the pair of components, the second current source being further configured to discharge the capacitive element when enabled.

21. The circuit of claim 20, wherein at least one of the clock drivers is responsive to a voltage at the capacitance to adjust the phase of its component clock signal.

22. A circuit comprising:

multiple components;

a plurality of clock drivers configured to provide separate clock signals to corresponding components by way of separate paths; and

a phase comparator corresponding to a pair of components, wherein the phase comparator receives the clock signals from each component of the pair of components and is responsive to the received component clock signals to generate a phase offset;

the clock drivers being responsive to phase offsets to synchronize the component clock signals at the components.

23. The circuit of claim 22, wherein a first component of the pair components comprises a first plurality of bit registers arranged in a first sequence and a second component of the pair components comprises a second plurality of bit registers arranged in a second sequence and wherein the clock drivers provide separate clock signals to each of the bit registers in each of the components of the pair of components via separate paths.

24. The circuit of claim 23, wherein the first and second components of the pair of components are located such that a first bit register of the second plurality of bit registers is located adjacent a last bit register of the first plurality of bit registers.

25. The circuit of claim 24, wherein the phase comparator receives the clock signals from the first bit register of the second plurality of bit registers and the last bit register of the first plurality of bit registers.

26. The circuit of claim 25, wherein the clock signals received by the phase comparator from the first bit register of the second plurality of bit registers and the last bit register of the first plurality of bit registers are routed on paths that are length matched.

27. The circuit of claim 22, wherein the clock signals are received at adjacent ends of the components.

28. The circuit of claim 22, wherein the component clock signals received by the phase comparator are routed from near the corresponding components.

29. The circuit of claim 22, wherein the separate paths have different propagation delays.

30. The circuit of claim 29, wherein the separate paths have different lengths.

31. The circuit of claim 22, wherein the phase offset is a digital phase offset.

32. The circuit of claim 22, wherein the phase offset is an analog phase offset.

33. A method of synchronous clocking, comprising:

routing separate clock signals to corresponding components;

comparing phases of clock signals received at a pair of component;

adjusting the clock signal received at one of the components to match the phase of the clock signal received at the other one of the components.

34. The method of claim 33, wherein the clock signals are received at adjacent ends of the components.

35. The method of claim 33, wherein the comparing comprises charging and discharging a capacitive element in response to the clock signals.

36. One or more components comprising:

means for routing individual clock signals to corresponding components;

means for comparing phases of clock signals received at a pair of components;

means for adjusting a clock signal from one of the components to match the phase of a reference clock signal; and

means for adjusting the clock signal received at one of the components to match the phase of the clock signal received at the other one of the components.